IN THE CLAIMS:

(WORKING FROM AMENDED SHEETS 26, 27 ANNEXED TO THE IPER)

Kindly substitute amended claims 1, 3-7, 9 and 11-15 for pending claims 1, 3-7, 9 and 11-15, and add new claims 16-18 as follows:

1. (Amended) A method of modifying a data model of an integrated circuit by electronic means, wherein the data model includes at least one layer of circuit components and wherein the method includes the steps of:

selecting a scaling factor,

scaling the entire circuit represented by the data model according to the scaling factor, and

adjusting each layer in the circuit for functionality and design rule compliance.

3. (Amended) A method according to claim 1, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

4. (Amended) A method according to claim 1, wherein the predetermined scaling ratios include the interconnect scaling ratio including geometry width and spacing for each routing layer, the via size ratio in each via layer and the transistor geometry ratio.

5. (Amended) A method according to claim 3, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

6. (Amended) A method according to claim 1, wherein the step of scaling the circuit according to the scaling factor includes multiplying the coordinates of the circuit geometry by the scaling factor.

92

~~7. (Amended) A method according to claim 1, wherein the step of~~ adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process whereby shapes in a sub-cell of the circuit may be scaled without breaking their connections with other parts of the circuit.

9. (Amended) A method according to claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

93

11. (Amended) A method according to claim 1, including the additional step of updating the contacts and vias by removing the existing contacts and vias and replacing them with new contacts and vias so as to reduce the current density through those contacts and vias.

12. (Amended) A method according to claim 1, including the step of adding and/or deleting layers in accordance with the target manufacturing process.

94

13. (Amended) A method according to claim 1, including the step of checking the circuit using a layout verification process.

14. (Amended) A method according to claim 1, including the preliminary step of analysing and modifying the circuit data.

15. (Amended) A method according to claim 1, including the step of adding a node containing design parameters to devices in the circuit.

16. (New) A method according to claim 2, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

17. (New) A method according to claim 4, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

95

18. (New) A method according to claim 16, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.